Paper code: ARI 304	L	T/P	Credits
Subject: Electronic Design Automation for VLSI	4	0	4

Marking Scheme:

Teachers Continuous Evaluation: As per university examination norms from time to time.

End Term Theory Examination: As per university examination norms from time to time.

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks: As per University Norms

1. There should be 9 questions in the end-term examination question paper
2. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be 15 marks.
3. Apart from Question No. 1, the rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, students may be asked to attempt only 1 question from each unit. Each question should be 15 marks.
4. The questions are to be framed keeping in view the learning outcomes of the course/paper. The standard/ level of the questions to be asked should be at the level of the prescribed textbooks.
5. The requirement of (scientific) calculators/log tables/data tables may be specified if required

Course Outcomes [Bloom's Knowledge Level (KL)]:

CO1: Students will understand and define various aspects of VLSI physical design and automation.**[K1,K2]**

CO2: The ability of students to understand the VLSI fabrication process. **[K1,K2]**

CO3: Illustrating the EDA simulator for circuit design and circuit simulation process. **[K3,K4]**

CO4: Understand , apply and analyze the layout designing of various VLSI circuits and devices. **[K2,K3,K4]**

CO/PO	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO1	3	3	2	3	3	0	0	0	0	1	0	3
CO2	3	3	2	3	3	0	0	0	0	1	0	3
CO3	3	3	2	3	3	0	0	0	0	1	0	3
CO4	3	3	3	3	3	0	0	0	0	1	0	3

Course Content	**No of Lectures**
Unit I **Physical Design Automation:** Basics of VLSI automation, Design cycle: system specifications, architectural, behavioural, logic, circuit, & physical design, fabrication, packaging, testing and debugging, new trends in VLSI design cycle: Increasing interconnect delay, increasing interconnect area, increasing number of metal layers, increasing planning requirements, logic synthesis, high-level synthesis, Physical design cycle: Partitioning, Floor-planning and Placement, Routing, Extraction and Verification, New trends in physical design cycle: chip level signal planning, OTC routing, Design Styles: Full custom, standard cell, Gate array, Field programmable gate array, sea of gates, Comparison of Different Design Styles.	[10]
Unit II **Carrier Transport Phenomena:** Fabrication materials, MOS architecture, Fabrication of	[10]

integrated circuits, material growth and oxidation: silicon dioxide, silicon nitride, Polycrystalline silicon, metals, doped silicon layers: diffusion & ion implantation, chemical mechanical polishing, Lithography: clean room, nMOS, pMOS fabrication steps, CMOS process flow, field oxide, shallow trench isolation.	
Unit III **Circuit simulator:** Simulator basics and type of simulators, historical perspective, circuit simulations: DC analysis: sweeping a source, the. dc statement, printing output, plotting output, graphics output, subcircuits, Ac analysis: specifying input source, Plotting bode plot, plotting group delay, input impedance, plotting output impedance, Noise analysis: the .noise statement, print and plot output, signal to noise, inserting noise source, Transient analysis: Simulating time, specifying input source, the . trans statement, graphic output and calculation, setting initial conditions, transient solution for static problems, distortion and spectral analysis: Fourier decomposition, the . four statement, large signal distortion, harmonic recomposition, intermodulation distortion.	[10]
Unit IV **Layout Simulation:** MOSFET Scaling and short channel effects, Layout design rules: micron & lambda rules: size rules, separation rules, overlap rules, Layouts of basic devices: nMOS, pMOS, Basic gate design: CMOS Inverter, NAND, NOR, Transmission Gate, Memory cells: 6T SRAM, DRAM. **Basics of EDA tools:** Layout and basics of simulators: Layout editor, Extraction, Design rule check, Layout versus schematic, placing, routing, Electrical Rule check, Lithography process check.	[10]

Textbooks:

[T1] Naveed Sherwani (2002) Algorithms for VLSI Physical Design Automation, Kluwer Academic Publishers
[T2] John P. Uyemura (2001) Introduction to VLSI Circuits and Systems, Wiley India.
[T3] Paul W. Tuinenga, (1993) SPICE A guide to circuit simulation and analysis using PSPICE, Prentice Hall.

Reference Books:

[R1] S. M. Sze (2017) VLSI Technology, 2nd Edition, McGraw Hill.
[R2] Kenneth S. Kundert () The designer's guide to SPICE and SPECTRE, Kluwer Academic Publishers.