Experiment :

Date 6/8/24

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Experiment-1

V-I Characteristics of a Diode

Site link - vlabs.iitkgp.ernet.in/be/exp5/index.html#

Aim - To study V-I characteristics of a diode

Apparatus - Fwd bias Si diode [1N4007], resistor, ammeter, etc

Theory - Structure of a P-N junction diode

The diode is a device formed from a function of n and p-type semiconductor material. Lead connected to p-type is anode and to n-type is cathode.

In fwd bias, diode +ve terminal of battery is connected to p side and -ve to n side. The holes in p-type and e^- in n-type are pushed towards junction reducing depletion zone width. In reverse bias, the depletion width increases.

Silicon - In order to conduct fwd biasing, voltage should be greater than the barrier potential it acts like closed switch with potential drop of 0.6V across. In reverse biasing depletion width increases and diode acts like open switch, thus is no current flow.

↳ The process is similar for Germanium diode, except that the potential drop is around 0.3V.

Diode Equation

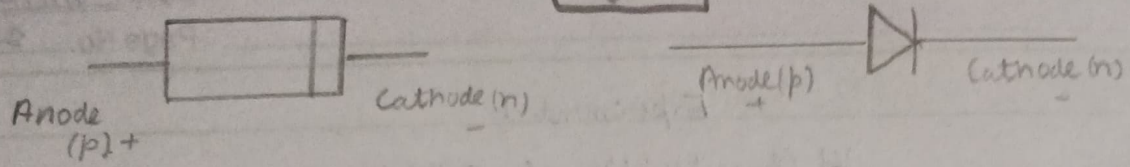
$$I_f = I_s \times \left(\exp \frac{V_f}{n \times V_T} - 1 \right)$$

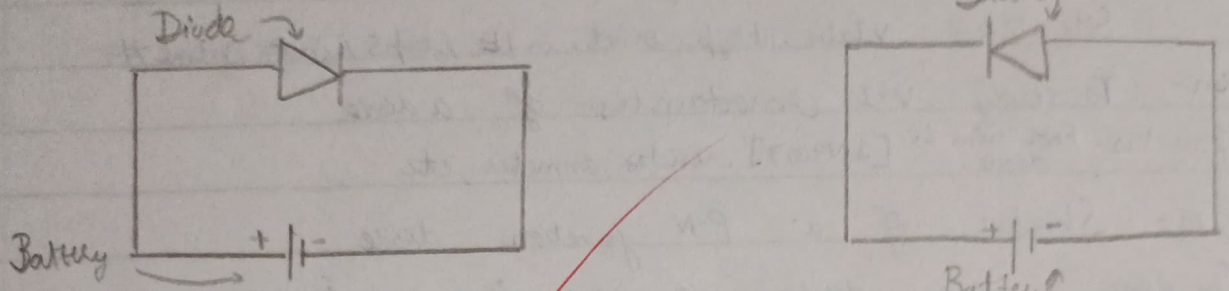
I_f : fwd current; I_s : leakage current; V_f : fwd voltage; V_T : thermal voltage

CLASSTIME

Diagrams →

Structure of P-N Junction Diode

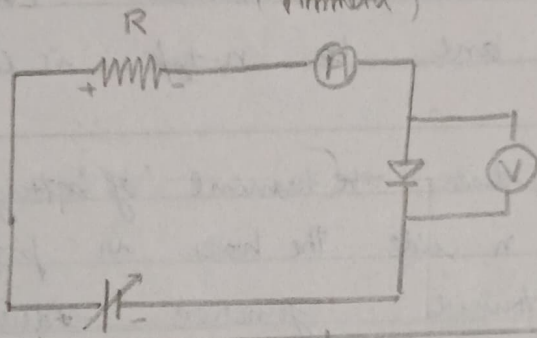




P-N junction diode function in (a) fwd bias (b) reverse bias

[FORWARD BIAS SILICON DIODE CKT Diagram]

R = 100Ω



→ Observation Table

S.No	$V_{Battery}$ (V)	V_R (V)	Forward Voltage (V)	Forward Current (mA)	IxR
1	0.6	0.6	0	0	0
2	0.7	0.172	0.528	0.0958	90.58
3	0.8	0.268	0.532	0.192	19.2
4	0.9	0.365	0.535	0.287	28.7
5	1	0.462	0.538	0.383	38.3
6	1.1	0.56	0.540	0.479	47.9
7	1.4	0.854	0.546	0.766	76.6
8	1.7	1.149	0.551	1.05	105
9	2.3	1.741	0.559	1.63	163
10	2.8	2.236	0.564	2.11	211

Experiment :

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Precautions -

1. Proper connection of the circuit (correct polarity, Tight connections)
2. Gradual variation of voltage, limiting current
3. Handling orientation of diode and avoiding overheating

Result / Conclusion -

1. When the forward bias voltage exceeds around 0.6V (cutoff voltage)
2. Current increases suddenly, when $V_R = 2.5V$ known as reverse breakdown.

R = 100Ω

(FORWARD BIAS SILICON DIODE)

S.No	$V_{Battery}$	V_R	Reverse Voltage (V)	Reverse Current (μA)	$V_R = I \times R$
1	0·2	0·3	0·170	0·1	10
2	1·3	0·12	1·18	0·1	10
3	3·7	0·22	3·48	0·1	10
4	5·7	0·26	5·44	0·1	10
5	6·95	0·28	6·6	0·1	10
6	9·15	0·29	8·86	0·1	10
7	11·7	0·30	11·4	0·1	10
8	14·3	0·20	14·1	0·1	10
9	17·95	0·15	17·8	0·1	10
10	20·3	0·10	20·2	0·1	10

V_R → Voltage across resistor
↳ $(V_B - V_D)$

R = 1000Ω

FORWARD BIAS

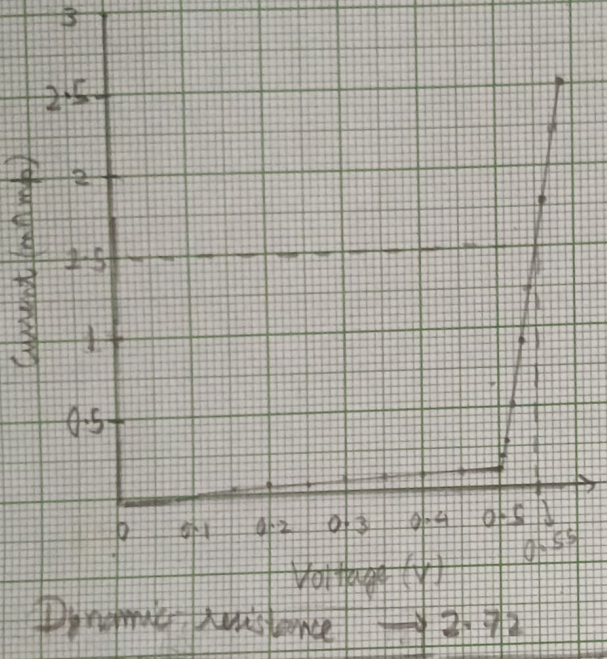
S.No	V_B (V)	V_D (V)	I_D (mA)	$V_R (V_B - V_D)$ (V)	V_R (I.R) (V)
1	0·2	0	0	0·2	0
2	0·7	0·630	0·1	0·17	0·1
3	1	0·539	0·4	0·461	0·4
4	1·3	0·546	0·7	0·714	0·7
5	1·6	0·051	1	1·049	1
6	1·9	0·555	1·3	1·345	1·3
7	2·2	0·588	1·6	1·641	1·6
8	2·5	0·866	1·9	1·937	1·9
9	2·8	0·566	2·2	2·234	2·2
10	3·1	0·571	2·8	3·129	2·8

V_B → Voltage of Battery
V_D → Voltage of Diode
I_D → Current of Diode
V_R → Voltage of resistor

FORWARD BIAS

SCALE
1 cm = 0.5 mA (Y-axis)
1 cm = 0.1 V (X-axis)

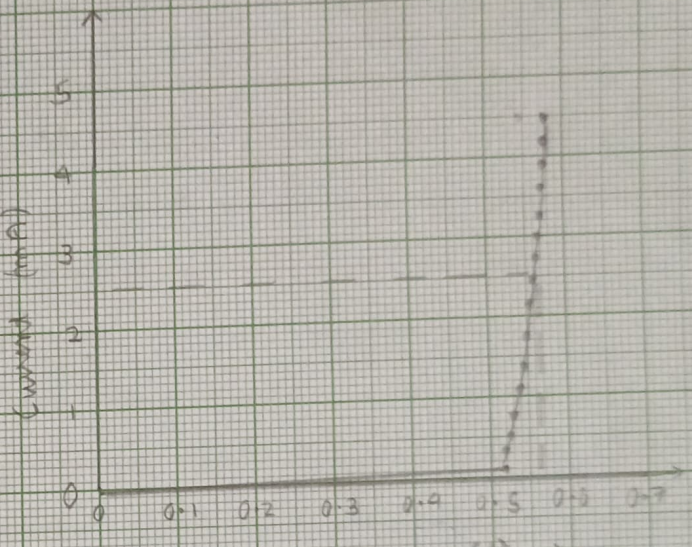
R = 100 Ω



Dynamic resistance → 2.72

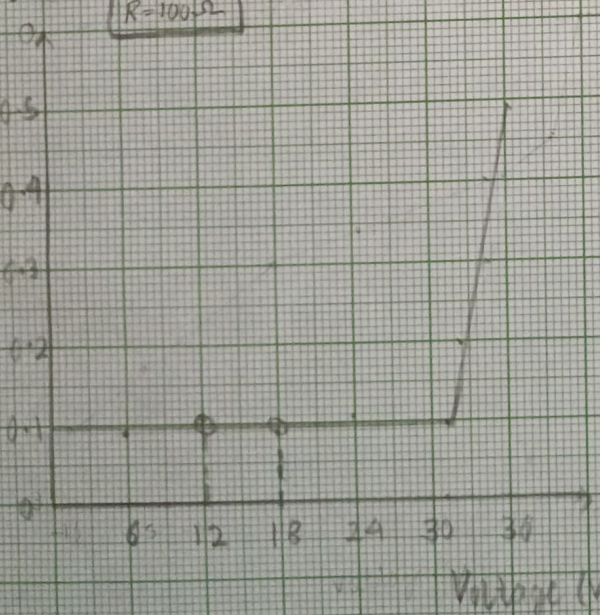
SCALE
1 cm = 1 mA (Y-axis)
1 cm = 0.1 V (X-axis)

R = 1 kΩ



REVERSE BIAS

R = 100 Ω



Dynamic resistance

$\frac{V_2 - V_1}{I_2 - I_1} = \frac{0.5 + 2 - 2}{0.5 - 0.3}$

$= 0.0209$

$\approx 19.2 \approx 20$

SCALE
① 1 cm = 0.1 mA (Y axis)
② 1 cm = 6 V (X-axis)

Dynamic Resistance

$Y = 0.1$

$\Rightarrow \frac{0.1 - 0.1}{18 - 12} \Rightarrow 0$

Experiment :

Date 28-8-24

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Experiment - 2

BJT Common Emitter Characteristics

Aim - To verify and find input and output characteristics of BJT Common emitter

Apparatus - BJT (BiPolar Junction Transistor), Resistor, connecting wires Ammeter (0-10mA, 0-100uA), DC power supply (0-30V), etc

(Site Link) - vlabs.iith.ac.in/be/exp11/index.html#

Theory - A BJT is a single piece of Si with 2 back to back PN junction BJT's can be made either as PNP or NPN They have 3 regions and 3 terminals emitter, base and collector - E, B and C. When Transistor is conducting normally, An easy way to remember is NPN stands for "Not Pointing IN"

Regions -

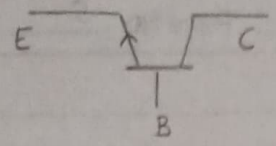
- Cutoff region - Base emitter junc^n is reverse biased, no current
- Saturation region - Base emitter is forward biased and collection biased junc^n is forward biased.
- Active region - Base emitter junc^n is forward biased, collector base junction is reverse biased.

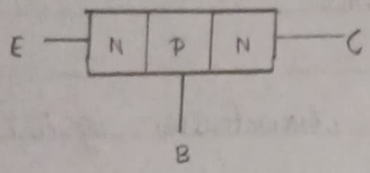
Breakdown region - I_c and V_{ce} exceed specifications and can cause damage to the transistor

Cutoff region - Both junctions are reverse biased $V_{BE} < 0$ (Base) and $V_{CB} > 0$ (with reverse biasing, all currents are zero.

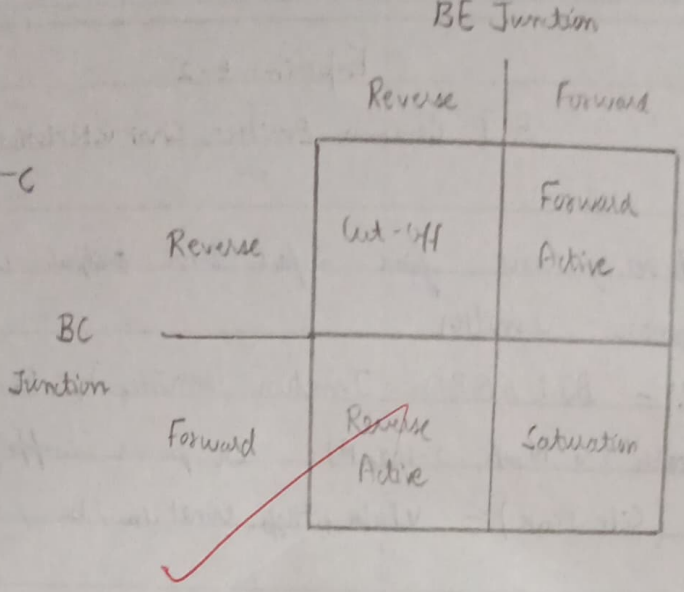
CLASSTIME

Structure of BJT

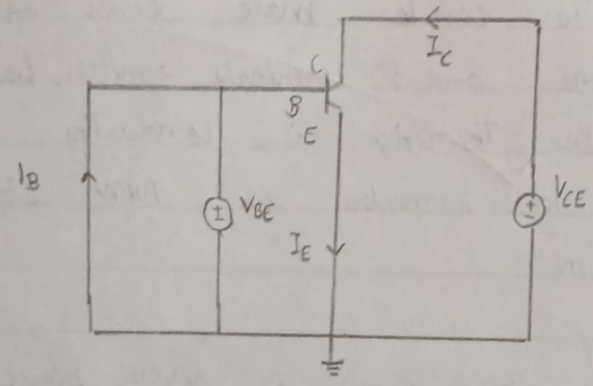




FOUR OPERATING CONDITIONS

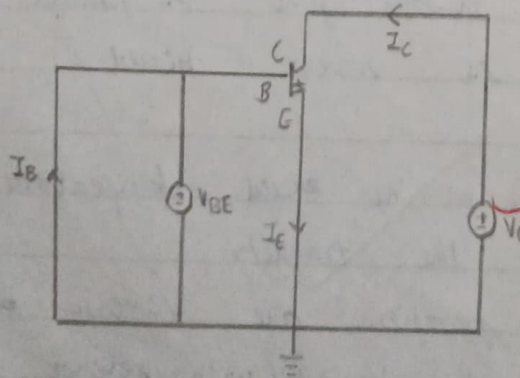


→ INPUT CHARACTERISTICS CKT



$I_B = \phi(V_{BE}, V_{CE})$ for constant V_{CE}

→ OUTPUT CHARACTERISTICS CKT



$I_C = \phi(V_{CE}, I_B)$ for constant I_B

Experiment :

Date

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Forward Active region-

Base is fwd biased ($V_{BE}<0$) and Collection is reverse biased ($V_{CB}<0$). fwd bias will cause injection of both hole and e^- across the junction.

$I_C = \alpha_F I_E + I_{CO}$, α is forward current transfer ratio

I_{CO} → collector reverse saturation current

Saturation region-

Both junctions fwd biased, Base is $V_{BE}>0$ and Collector-Base is $V_{CB}<0$. Max current flow through transistor, only small voltage drop.

Reverse active region

Base-emitter is reverse biased ($V_{BE}<0$) and collector base is fwd biased ($V_{CB}<0$). Current gain is smaller.

Application- In digital circuits and analog switching circuits

$I_E = -\alpha_R * I_C + I_{EO}$

α_R → reverse current transfer ratio

I_{EO} → Emitter reverse saturation current

BJT - Common Emitter Circuit

↳ described as Ebers-Moll Model -

$I_F = I_{ES} \times \left(\exp \frac{V_{BE}}{V_T} - 1\right)$

$I_R = I_{CS} \times \left(\exp \frac{V_{CB}}{V_T} - 1\right)$

I_{ES} → base-emitter saturation current

I_{CS} → base-collector saturation current

CLASSTIME

(A)

S.No	Base emitter Voltage (V)	Base current (uA)	$Rh_1(\Omega)$
1	0.2	2.824	10
2	0.3	3.232	15
3	0.4	3.704	20
4	0.5	4.248	25
5	0.6	4.875	30
6	0.7	5.599	35
7	0.8	6.434	40
8	0.9	7.397	45
9	1	8.508	50
10	1.1	9.784	55
11	1.2	11.27	60
12	1.3	12.97	65
13	1.4	14.94	70
14	1.5	17.21	75
15	1.6	14.83	80

(a) $V_{CE} = 1V$
$Rh_2 = 10\Omega$

(Const)
[$Rh_2 = 10\Omega$
CE Voltage $= 10V$]

INPUT CHARACTERISTICS

(B)

S.No	Base emitter Voltage (V)	Base current (mA)	$Rh_1\ \Omega$
1	0.02000	2.077	10
2	0.08000	2.261	15
3	0.1900	2.462	20
4	0.2000	2.680	25
5	0.2600	2.918	30
6	0.3200	3.178	35
7	0.3800	3.461	40
8	0.4400	3.769	45
9	0.5000	4.104	50
10	0.5600	4.470	55

(b) $V_{CE} = 2V$
$Rh_2 = 20\Omega$

Experiment :

Date

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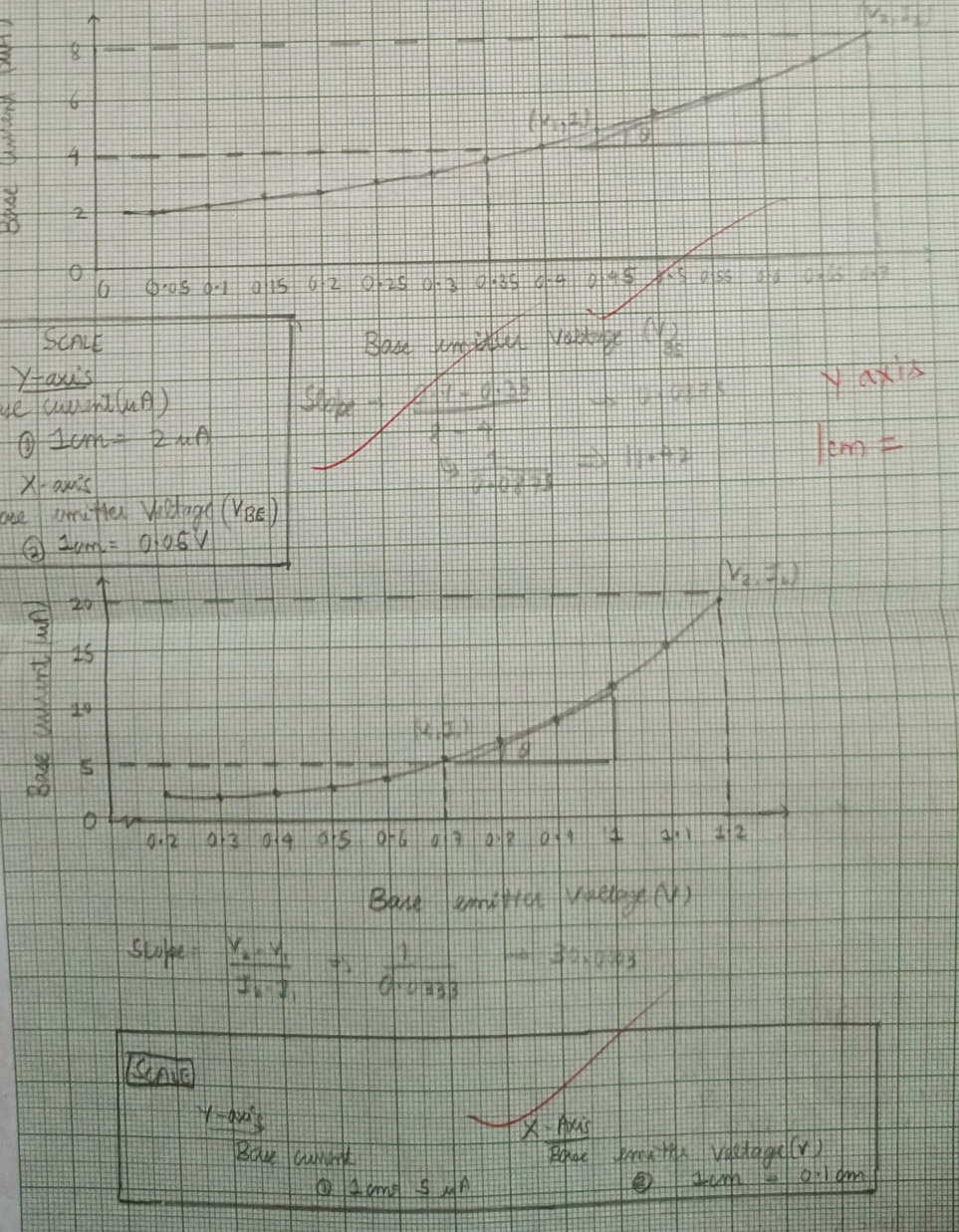
Precautions

1. Ensure proper connection and biasing.
2. Check polarity and avoid overheating
3. Calibrate instruments and avoid static discharge

Result -

The characteristic behaviour of BJT in various regions such as active, saturation etc is shown.
It may be helpful to design circuits involving BJT like - amplifiers and switches.

INPUT CHARACTERISTICS (V-I PLOT)



(A)

S.No	Output Emitter Voltage (V)	Collector Current (mA)	Rh_2 (Ω)
1	1	1750	10
2	1.5	2080	15
3	2	2215	20
4	2.5	2267	25
5	3	2286	30
6	3.5	2293	35
7	4	2298	40
8	4.5	2297	45
9	5	2297	50
10	5.5	2297	55
11	6	2298	60
12	7	2298	65
13	7.5	2298	70
14	8	2298	80

(A) $I_b = 15.35$
$Rh_1 = 15$

OUTPUT CHARACTERISTICS

(curve)

$Rh_1 = 100\,\Omega$
Base-current
174.14 mA

(B)

S.No	Collector emmitter Voltage N)	Collector Current(mA)
1	0.1000	7.427
2	0.4000	35.08
3	0.7000	55.80
4	1.000	70.31
5	1.300	79.86
6	1.600	85.09
7	1.900	88.28
8	2.200	91.08
9	2.500	91.09
10	2.800	91.64

(B) $I_b = 20.43$
$Rh_1 = 25$

(I_b → Base current)

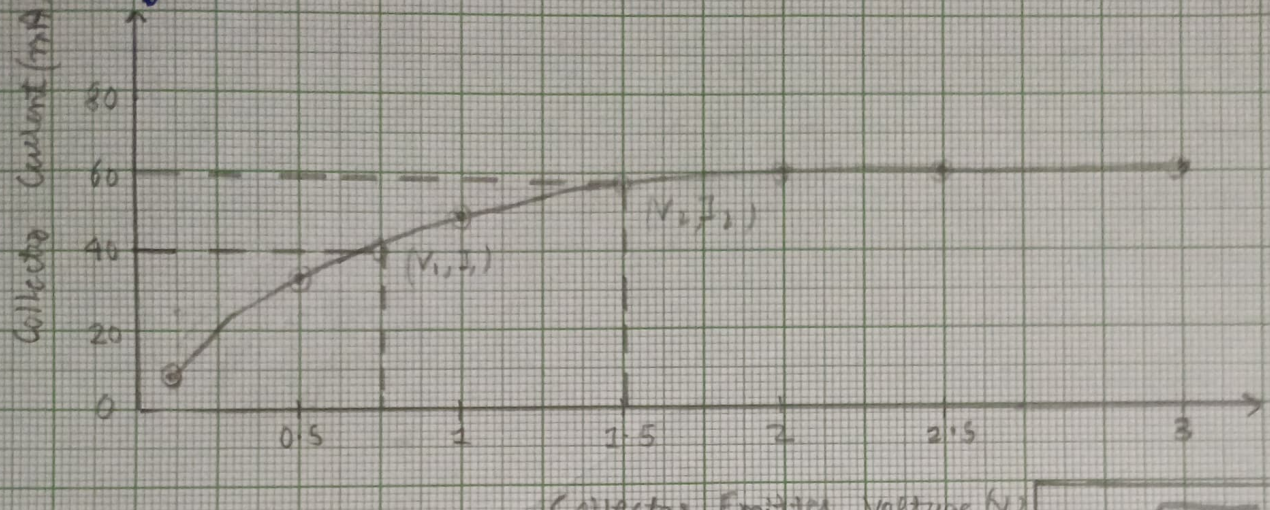
(C)

S.No	Collector emitter Voltage N)	Collector Current (mA)
1	0.1000	12.96
2	0.4000	49.42
3	0.7000	78.62
4	1.000	99.07
5	1.300	112.1
6	1.600	119.9
7	1.900	124.4
8	2.200	126.9
9	2.500	128.3
10	2.800	129.1
11	3.100	129.6
12	3.400	129.8

(C) $I_b = 25.67$ $Rh_1 = 33$

CHARACTERISTICS (V-I PLOT)

(A)



Slope = $\frac{60-0}{1.5-0.75} = 80.00$

SCALE

Y-axis

Collector Current

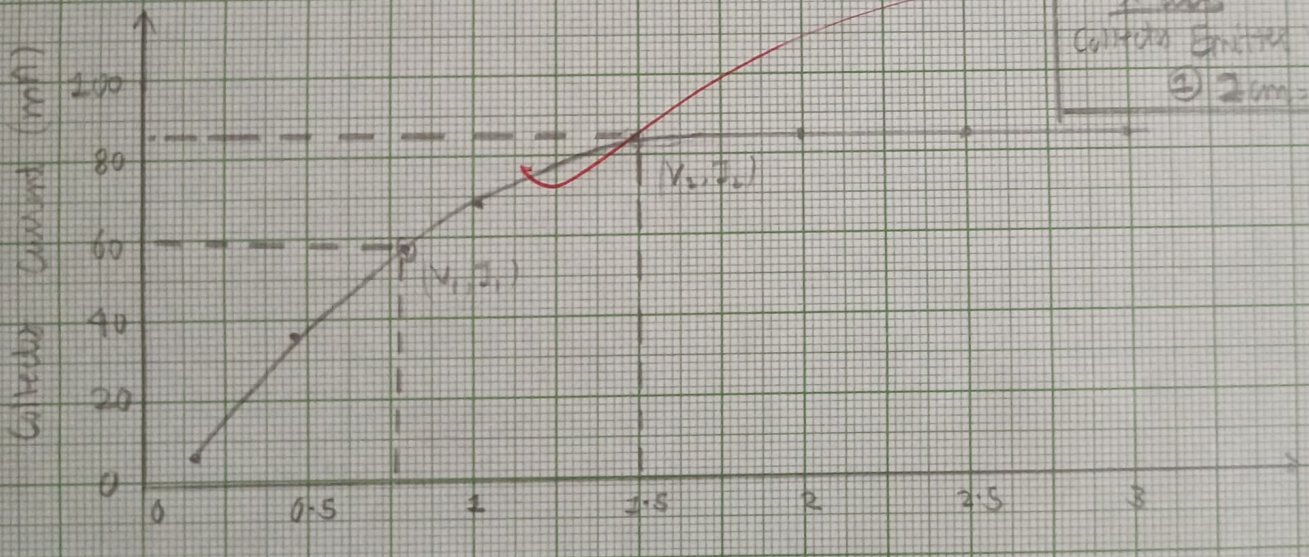
① 1cm = 20 mA

X-axis

Collector Emitter Voltage

① 2cm = 0.5V

(B)



Slope : $\frac{I_2 - I_1}{V_2 - V_1}$

$\rightarrow \frac{80-60}{1.5-0.75}$

$\rightarrow \frac{20}{0.75}$

$\rightarrow 26.666$

SCALE

Y-axis

Collector Current

1cm = 20 mA

① X-axis

Collector Emitter voltage

② 2cm = 0.5V

Experiment :

Date 10/9/24
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Experiment - 3
Full Wave Rectification

Aim- To study full wave rectification

Apparatus- Oscilloscope, resistor (R_L), connecting wires

Theory-

Rectification - Device that convert AC to DC. It's of 2 types- a half wave and a full wave rectifier

① Full Wave Rectifier

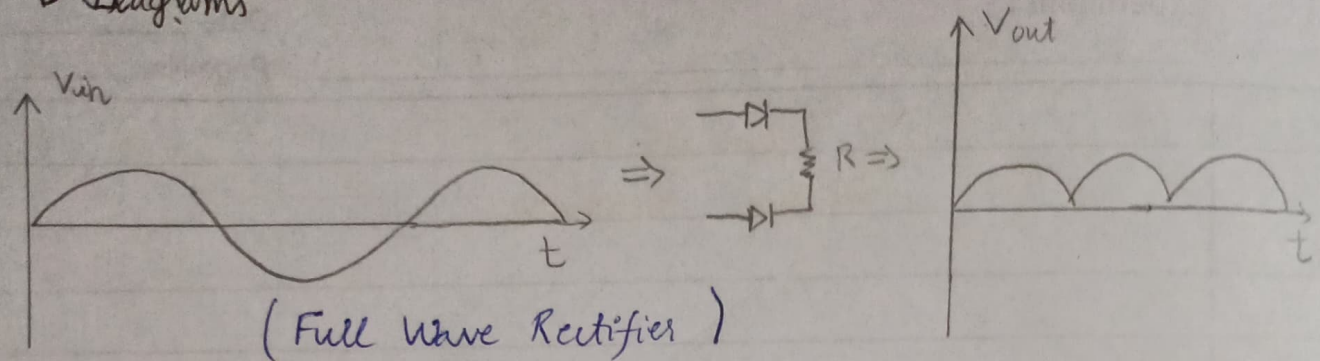
It's exactly the same as half-wave but allows unidirectional current through the load during entire sinusoidal cycle. It converts the whole of the input waveform to one of constant polarity (positive or negative) at its input

② Centre Tapped Transformer

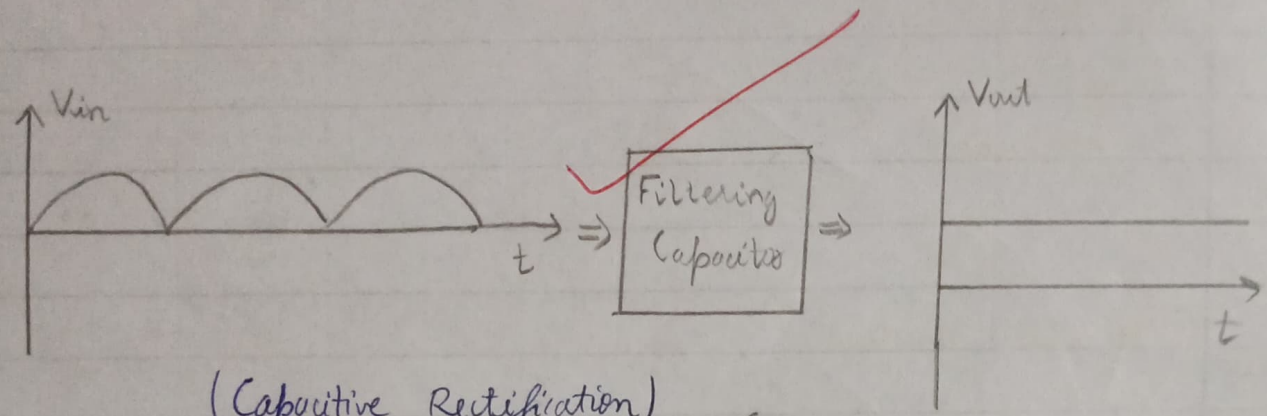
A full wave rectifier can be constructed using centre Tapped transformer. Gives us two shifted sinusoids so exactly one of the waveform is positive at one time. Allows for conduction through load.

CLASSTIME

→ Diagrams

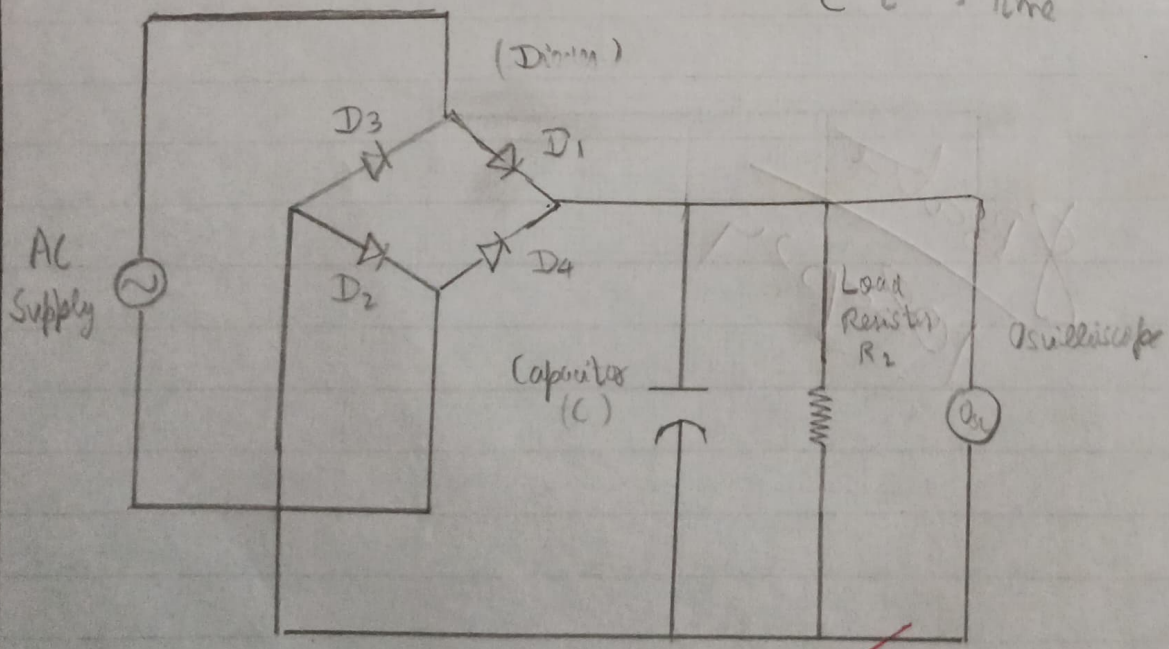


(Full Wave Rectifier)



(Capacitive Rectification)

{ Vin → Vinput (Input voltage)
Vout → Voutput (output voltage)
t → Time }



Ckt diagram for full wave rectifier with filtering

Experiment :

Date

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(B) Bridge Rectifier

It uses 4 rectifying diodes connected in a bridged config. to produce desired output that doesn't require special tapped transformer thereby reducing reducing cost and size.

Avg DC Load Voltage = $V_{DC} = \frac{2V_m}{\pi}$

Avg. Load Current = $\frac{2 \times I_m}{R}$

RMS Load Current = $\frac{I_m}{\sqrt{2}}$ RMS Load Voltage = $\frac{V_m}{\sqrt{2}}$

Form factor = $\frac{\pi}{2\sqrt{2}} = 1.11 \rightarrow \frac{V_m/\sqrt{2}}{2V_m/\pi}$

(2) Capacitive Rectification

↳ Capacitive Rectification - A full wave rectifier converts the whole of input waveform to one of constant polarity at its output. But what is really desired to convert pulsating output of rectifier to a constant dc supply, thus filter input signal

↳ The simplest kind of filter that can perform filtering taste is a capacitor. When connected, the AC components will have a low impedance path to ground and not appear in output.

CLASSTIME

→ Observation Table

Amp → Amplitude / mV

1. Full Wave Rectifier

(a) Set 1
freq = 1000Hz
R_L = 500Ω

(b) Set 2
freq = 1000Hz
R_L = 400Ω

(C) Set 3
freq = 1000Hz
R_L = 300Ω

(A)

S.No	Amp(V)	Peak current (mA)
1	0	-1.4
2	0.5	-0.400
3	1	0.799
4	1.5	1.599
5	2	2.59

(B)

S.No	Amp(V)	Peak Current (mA)
1	0	-1.74
2	0.5	0.71
3	1	0.74
4	1.5	1.749
5	2	2.749

(C)

S.No	Amp(V)	Peak Current (mA)
1	0	-2.33
2	0.5	-0.66
3	1	0.91
4	1.5	2.33
5	2	4.33

Experiment :

Date

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Ripple Voltage and Ripple Factor

A new charging pulse occurs every half cycle the capacitor charges and discharges very quickly The variable portion is known as ripple Further ratio of ripple voltage to avg. voltage is ripple factor.

↳ Precaution

1) Check the capacitor polarity
2) Monitor ripple voltage voltage across load.
3) Ensure proper Oscilliscope probing
4) Check diode Orientation and connection

↳ Conclusion

↳ In this experiment, using a bridge rectifier with 4 diodes, both halves of AC waveform into pulsating DC output. Bridge rectifier provides a more efficient rectification proves by utilizing entire AC cycle. The inclusion of capacitor reduced ripple in rectified output resulting in a constant DC voltage.

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23/9/24

CLASSTIME

(2) Capacitive Rectification

$V_{pp_1} = 1V$
Position Y-axis = 0.1
Phas = 0 deg
Freq = 1000Hz

$V_{pp_2} = 1V$
Position X-axis = 0.1
Phase = 0 deg
freq = 1000Hz

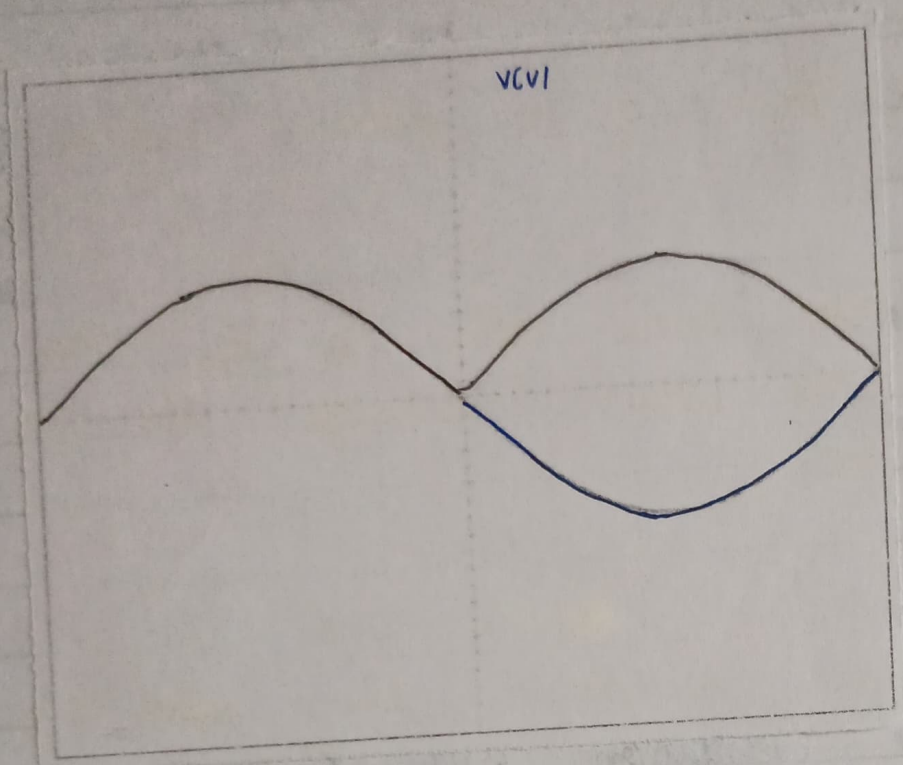
Oscilloscope Least Count = 0.01 (for Voltage)
1 ms (for time)

→ Calculations

Form factor = $\frac{V_{rms}}{V_{avg}} \Rightarrow \frac{V_m/\sqrt{2}}{2V_m/\pi} \Rightarrow \frac{\pi}{2\sqrt{2}} = 1.11$

Ripple Factor $\Rightarrow \gamma \Rightarrow \sqrt{(\text{Form factor})^2 - 1)} \times 100\%$
↳ 48.1 %

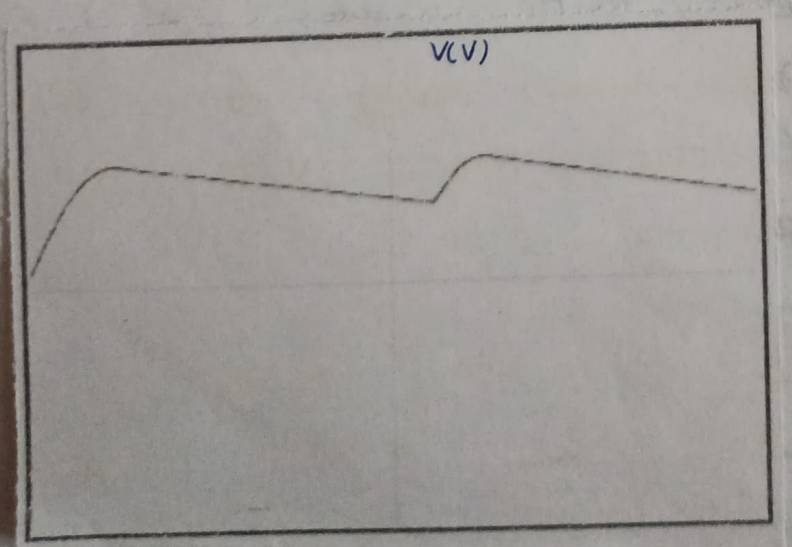
(a) Full Wave Rectifier



Black line represents rectified output DC and blue line represents input AC

frequency = 1000 Hz
Amplitude = 1 V
R_L = 500 Ω
(Load resistance)

(b) Capacitive Rectification



Rectified Output DC

frequency = 1000 Hz

Experiment :

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Experiment - 4
Half Wave Rectifier

Aim - To study half wave rectification

Apparatus - Oscilloscope, connecting wires, resistor, diode, AC supply,

Theory
Rectifier is a device that converts AC to DC, process known as rectification

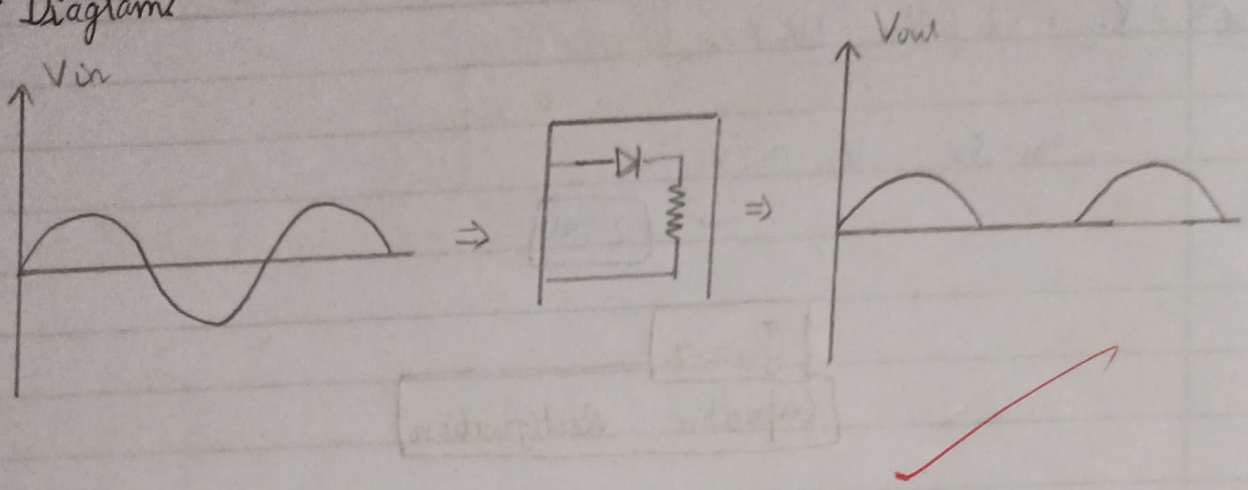
Half Wave Rectification
On the positive cycle diode is is forward biased and on negative cycle diode is reverse biased. Using diode, AC source is converted into a DC source, Half wave rectifier is a circuit that allows only part of an input signal to pass and single diode is in series with resistor (load).

↳ For positive half cycle -
Acts as a short circuit -

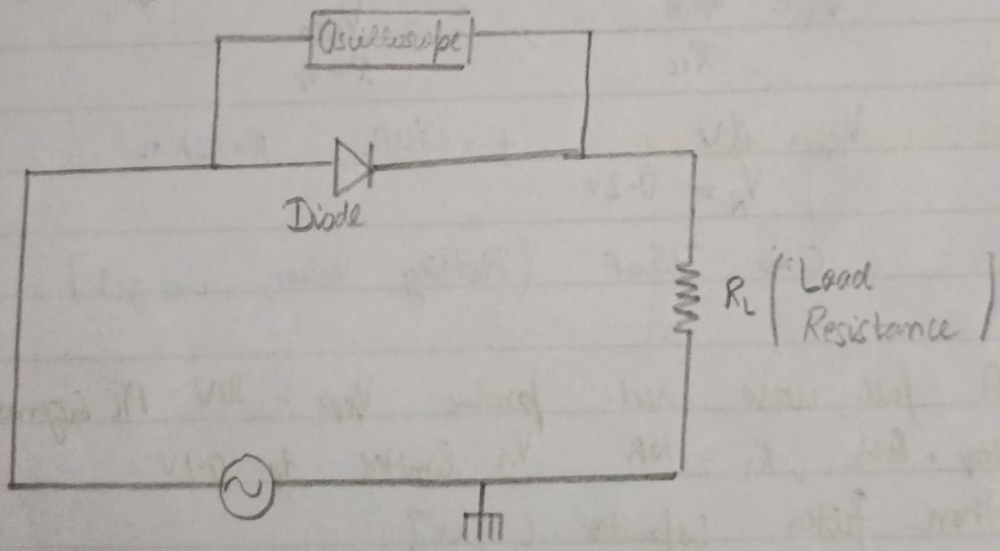
$$V_I - V_b - I \times r_d + I \times R = 0$$

V_I : Input voltage
V_b : Barrier Voltage
r_d : diode resistance

→ Diagram



↳ Circuit Diagram



$V_0 = I \times R \quad = V_I = \frac{V_b}{r_b + R} \times R$

$V_0 = V_1 - V_b$

↳ For negative half cycle

Acts as open circuit

$V_0 = 0$ V since $I = 0$

Average output voltage $= \frac{V_m}{\pi} = 0.318\ V_m$

RMS Voltage Load $= \frac{V_m}{2}$

↳ Peak Inverse Voltage

It is the max value of reverse voltage which occurs at peak of input cycle when diode is reverse biased.

$PIV = V$

$-V_m + V = 0 \Rightarrow V = V_m \; ; \; PIV \geq V_m$

↳ Precautions

1) Ensure proper grounding
2) Observe ripple, ensure oscillator is sensitive enough to detect ripple voltage
3) Avoid overheating

Observation Table

(a) Set 1
freq = 3000 Hz
R_L = 100 Ω

(b) Set 2
freq = 3000 Hz
R_L = 200 Ω

(c) Set 3
freq = 3000 Hz
R_L = 300 Ω

(A)

S.No	Amp(V)	Peak Current (mA)
1	0	-6.99
2	0.5	-2.00
3	1	1.99
4	1.5	6.99
5	2	12.99

(B)

S.No	Amp(V)	Peak Current (mA)
1	0	-3.99
2	0.5	-1.00
3	1	1.48
4	1.5	3.99
5	2	5.99

(C)

S.No	Amp(V)	Peak Current (mA)
1	0	-2.33
2	0.5	-0.66
3	1	0.99
4	1.5	2.33
5	2	4.33

Calculations

Form factor (F.F.)

↳ $\frac{V_{rms}}{V_{avg}}$

↳ $\frac{V_m/2}{V_{av}/2} \Rightarrow \frac{\pi}{2} = 1.57$

Ripple factor

$\gamma = \sqrt{(F.F.)^2 - 1} \times 100\%$

↳ 1.21 %

Experiment :

Date

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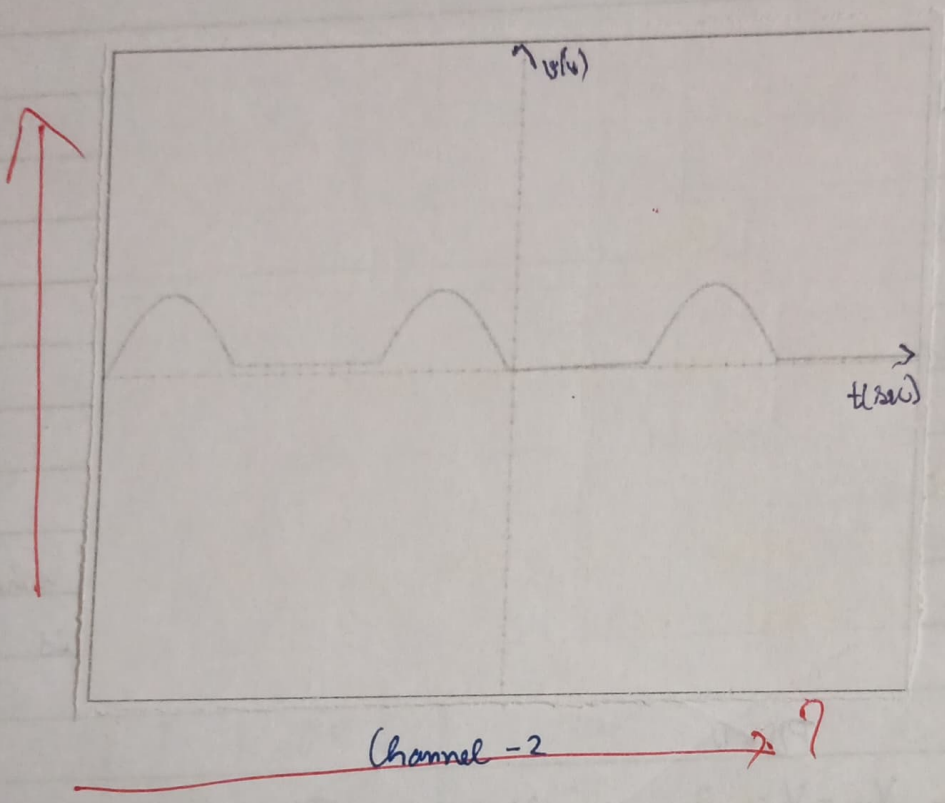
Conclusion

In half wave rectifier o/p, AC converts into pulsating DC output. Only one half of AC cycle is utilized while the other ~~half~~ is blocked by diode resulting in significant amount of ripple in output.

Graph

Half Wave Rectification



Rectified Output DC

f (frequency)

freq → 3000 Hz

R_L → 200 Ω

(↳ Load resistance)

Amp = 1.5V

↳ (Amplitude)

Oscilloscope Least Count = 0.01 V (for voltage)

= 1 ms (for time)

Experiment :

Date 17/9/24
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Exp 5

BJT CE Amplifier

Aim- To study BJT CE Amplifier

Apparatus- Capacitor, resistor, transistor, connecting wires, Input AC

Theory- The CE configuration is widely used as a basic amplifier as it has both voltage and current amplification. R_{B1} and R_{B2} form voltage divider across base of transistor. Biasing done such that Q point is in active region

→ Bypass capacitor

The emitter resistor R_E is req to obtain DC Q point stability. Bypassed by a capacitor so that it acts as a short circuit for AC. Capacitor is connected in parallel.

$$X_{CE} \ll R_E$$

$$C_E \gg \frac{1}{2\pi f R_E}$$

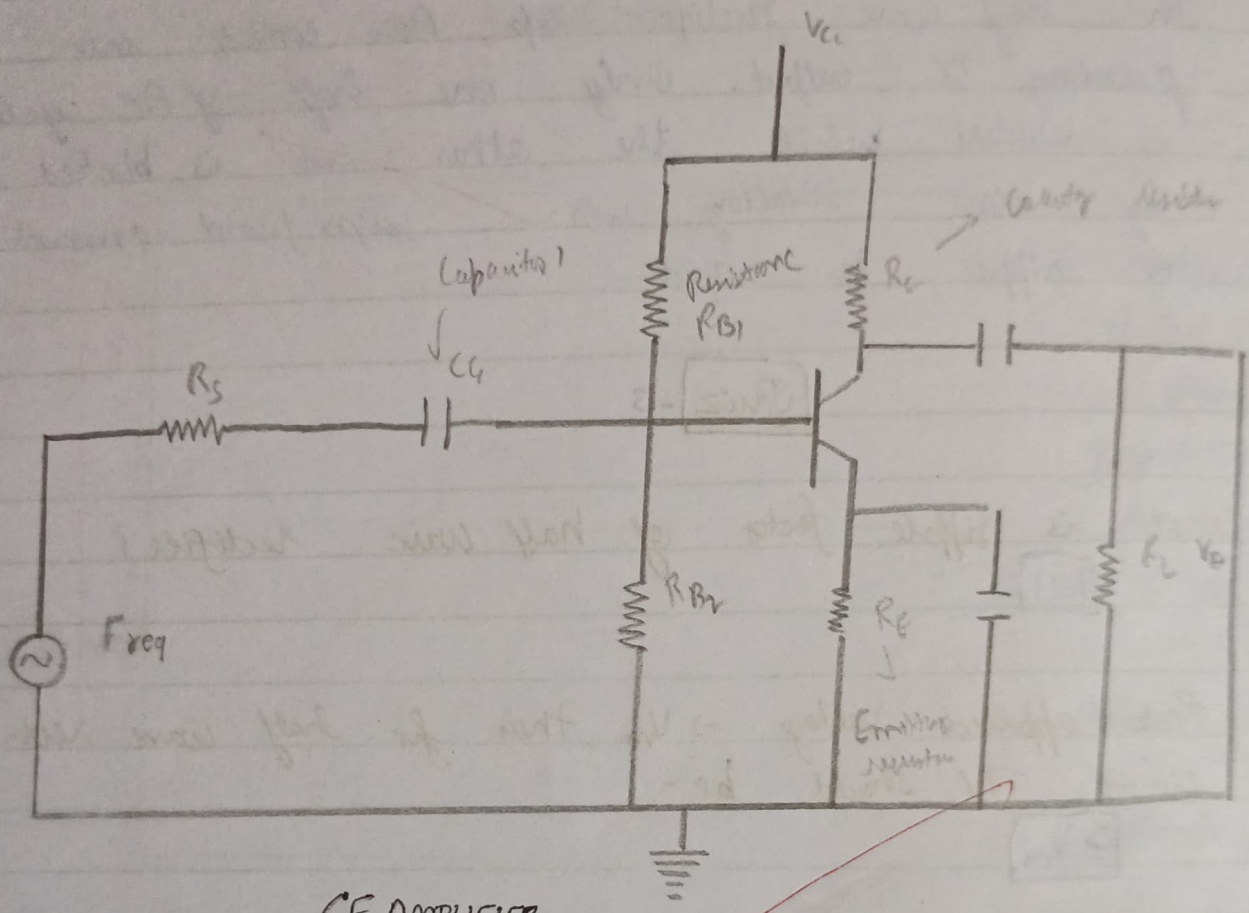
In order to have noiseless transmission of a signal DC shouldn't enter load. Accompanied by coupling capacitor.

→ Frequency response of CE Amplifier

Emitter bypass cap are used to short circuit and thus increase gain at high frequency. Stray capacitances are

CLASSTIME

→ DIAGRAM-



CE AMPLIFIER

Experiment :

Date

Page No.

effectively open circuits. Hence, the mid band frequency gain is maximum. At high frequencies, bypass and coupling capacitors are replaced by short circuits

$$A_{(s)} = \frac{A_m \times s^2 \times (s+\omega_{z1})}{(s+\omega_{p1}) \times (s+\omega_{p2}) \times (s+\omega_{p3})}$$

→ Precaution -

1. Ensure proper biasing of transistors
2. Use proper capacitor values for coupling and bypassing
3. Limit input signal amplitude and avoid short circuits

→ Conclusion

The BJT CE amplifier demonstrates how biasing and component selection affect amplifier's voltage gain, input / output characteristics and overall performance proper biasing ensures transistor operates in active region achieving desired amplification

※ Observation

Constants- $R_S = 100\,\Omega$, $C_{C_1} = 10\,\mu F$, $R_{B_2} = 10000\,\Omega$
$R_{B_1} = 47000\,\Omega$, $R_L = 4000\,\Omega$, $R_{CE} = 1000\,\Omega$, $C_{C_2} = 10\,\mu F$
$C_E = 10\,\mu F$, $R_L = 2000\,\Omega$

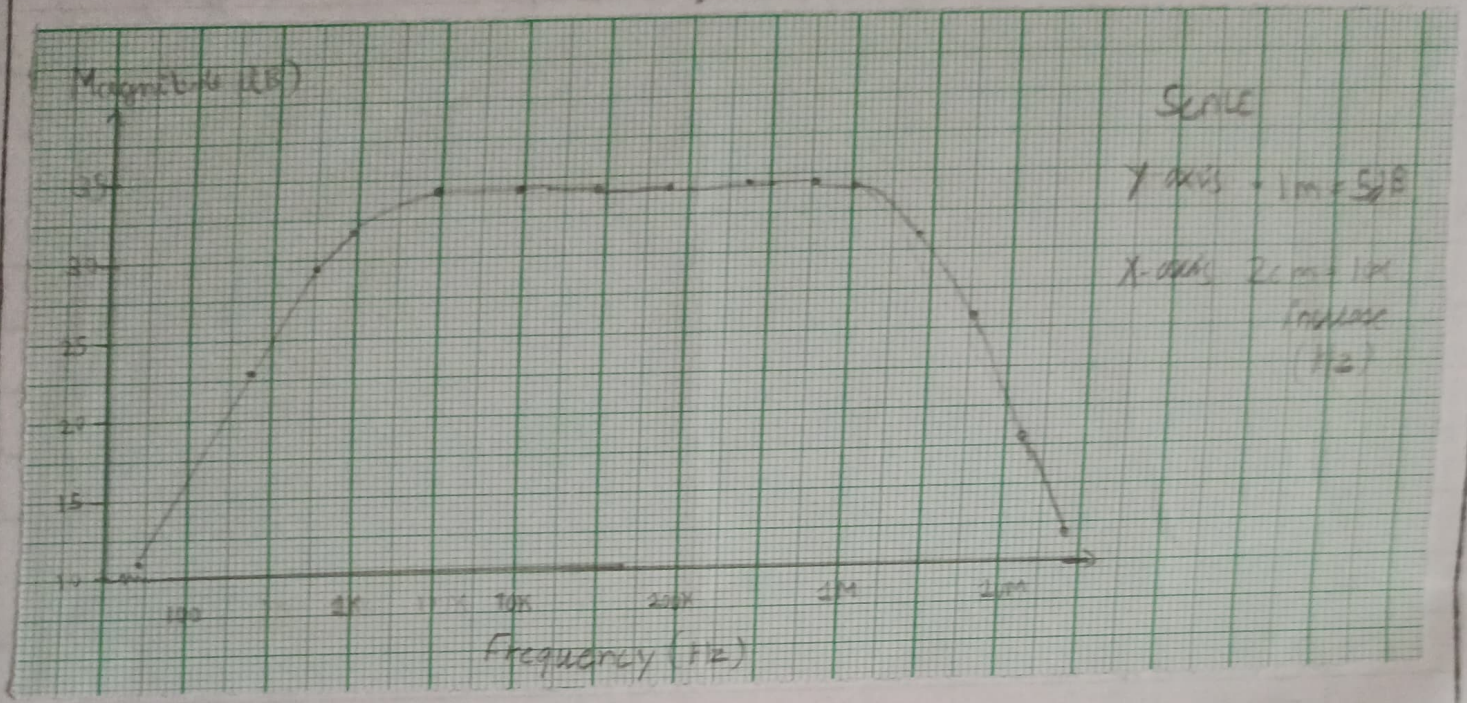
S.No	Frequency (Hz)	Magnitude (dB)
1	50	10.591
2	220	22.813
3	552	29.4378
4	959	32.0726
5	2896	34.065400000004
6	8746	34.3512
7	20036	34.368400000004
8	87462	34.3814
9	182734	34.376
10	418620	34.2238
11	1105130	33.9941
12	2641310	32.3504
13	7976646	26.28499
14	18273400	19.66136
15	50329200	10.99534

Midband gain = -52.4119

Low freq. cut off = 5058.95931 3745 Hz

High freq cutoff = 2.1455E + 7 Hz

⇒ GRAPH :-


Magnitude (dB)
30
25
20
15
10
100
1K
10K
100K
1M
10M
Frequency (Hz)
SCALE
Y axis : 1cm = 5dB
X axis : 2cm = 1M
Increase (Hz)

Experiment :

Date 24/9/24

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Experiment-6

Astable and Monostable Multivibrator using IC 555

Aim- To study astable and monostable multivibrator using IC 555

Theory- Multivibrator is electronic ckt used to implement 2 state systems like flip flops, timers, classified into-3 types - ① Monostable
② Astable
③ Bistable

A bistable multivibrator ckt is stable that can be changed from one state to another by external trigger pulse
Also called flip-flop

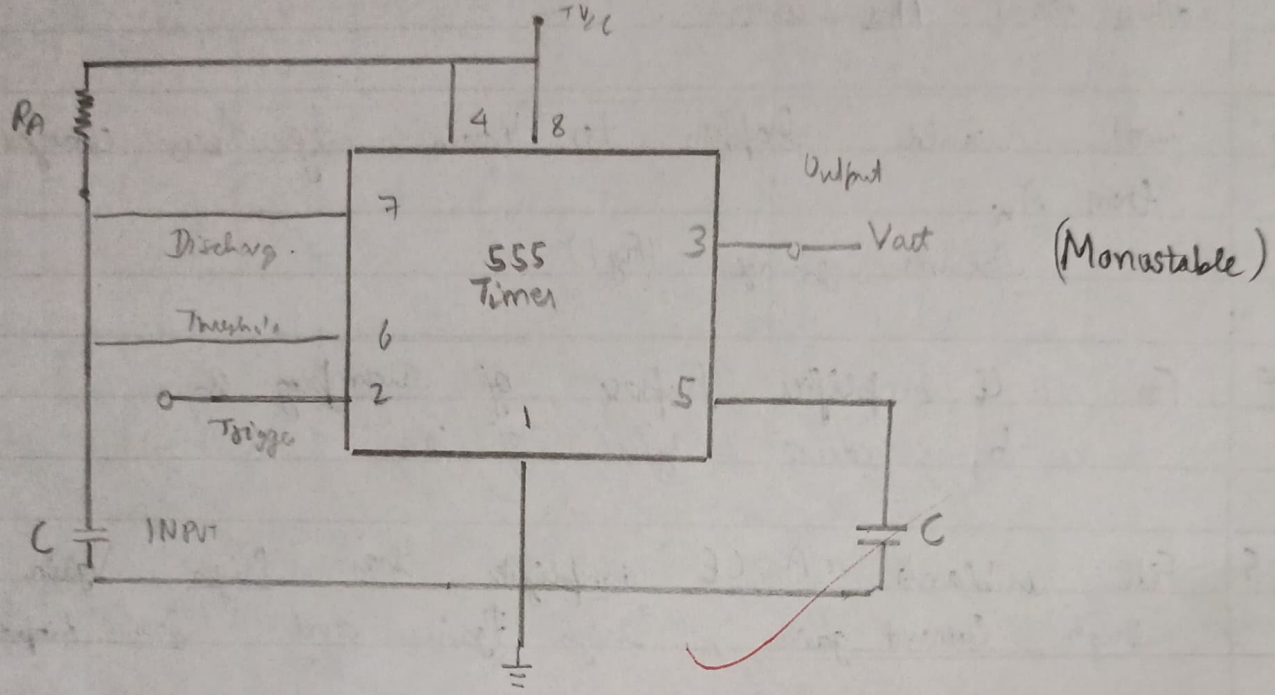
① Monostable multivibrator
They have only one stable state that is used to generate singe o/p pulse of specified width value when external trigger applied. It will continue in this state till another i/p is required. produces much longer rectangular waveform.

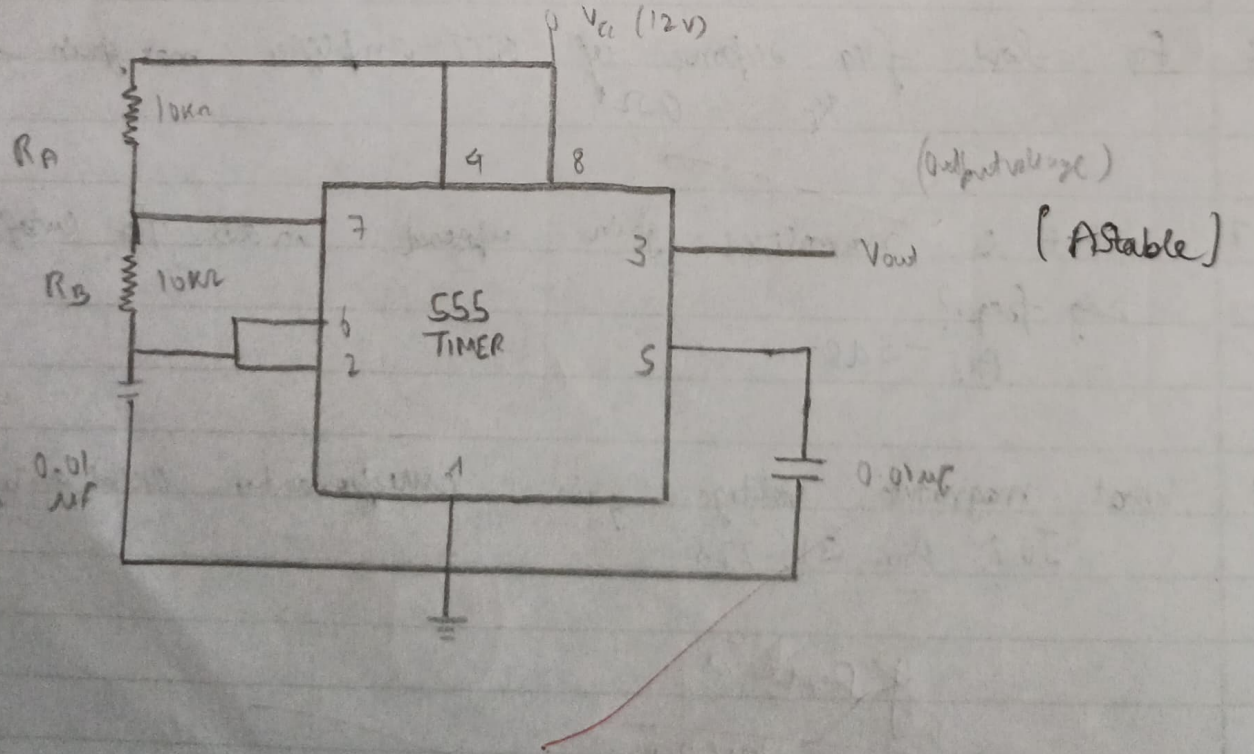
Time duration (T) = RC x 1.1

It only needs one single pulse to start and constructed easily, less price Used in storage ckt.

CLASSTIME

⇨ Diagram


+V_CC
RA
4
8
7
Discharg.
555
Timer
3
Output
Vout
(Monostable)
Threshold
6
2
Trigge
1
5
C
INPUT
C


V_CC (12V)
10KΩ
RA
4
8
(Output voltage)
7
3
Vout
(AStable)
RB
10KΩ
555
TIMER
6
2
5
0.01
μF
1
0.01μF

Experiment :

Date

Page No.

② Astable Multivibrator

Also known as free running / alternatives between output voltage levels, It is a multivibrator in which circuit isn't stable in either state, It continually switches from one state to another.

$$T = 0.693 * (R_1 + 2R_2) C_1$$

$$f = 1/T$$

Duty cycle (ratio of time for which output is high to total time) :-

$$\frac{T_1}{T} \times 100 = \frac{R_1 + R_2}{R_1 + 2R_2} \times 100$$

↳ Apparatus - 555 timer IC, Connecting wires, oscilloscope, resistor, Capacitor, breadboard.

↳ Precautions :-

1. Ensure supply voltage doesn't exceed in 555
2. Ensure capacitor discharges properly
3. Ensure IC doesn't overheat

↳ Conclusion - Behaviour of both multivibrators were demonstrated Astable generated a continuous square wave while monostable produced single pulse in response to trigger

CLASSTIME

* Observation Table

① Monostable (V_{cc} = 12V, R_A = 10KΩ, C = 0.01μF)

S.No	R(KΩ)	Capacitance (μF)	Pulse width (msec)	Duty Cycle (D%)
1	70	0.01	1.1	11
2	30	0.01	3.3	33
3	50	0.1	5.5	55
4	70	0.1	7.7	77

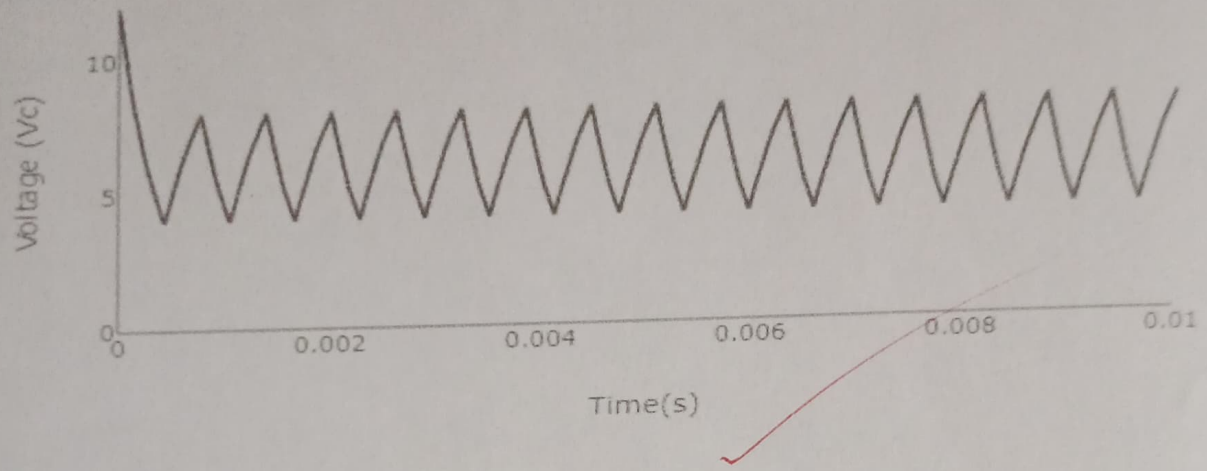
[Least Count = 1 milisecond]

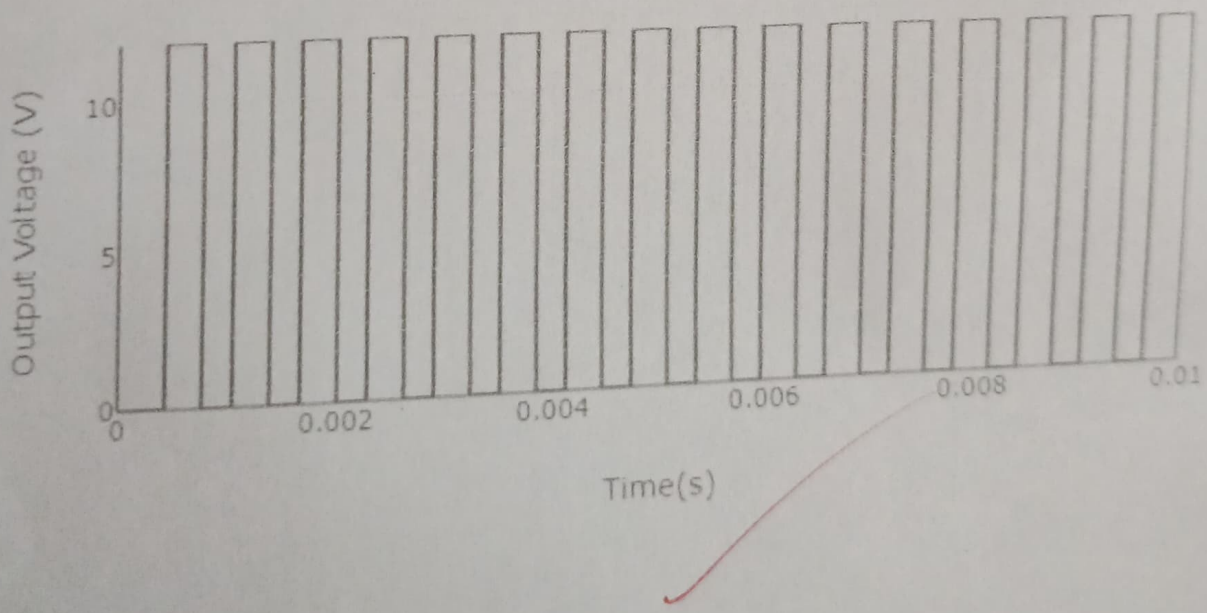
② Astable (V_{cc} = 12V, $R_H = R_B$ = 10KΩ, C = 0.01μF)

S.No	R_A (KΩ)	R_B (KΩ)	C (μF)	Pulse width (Tp msec)	T (msec	D%	Freq (Hz)
1	1	3.9	0.1	0.338	0.607	55.68	1.65
2	3	3.9	0.1	0.476	0.795	63.89	1.34
3	5	3.9	0.1	0.614	0.683	69.53	1.13
4	7	3.9	0.1	0.752	1.026	73.65	0.88
5	9	3.9	0.1	0.890	1.159	76.99	0.66

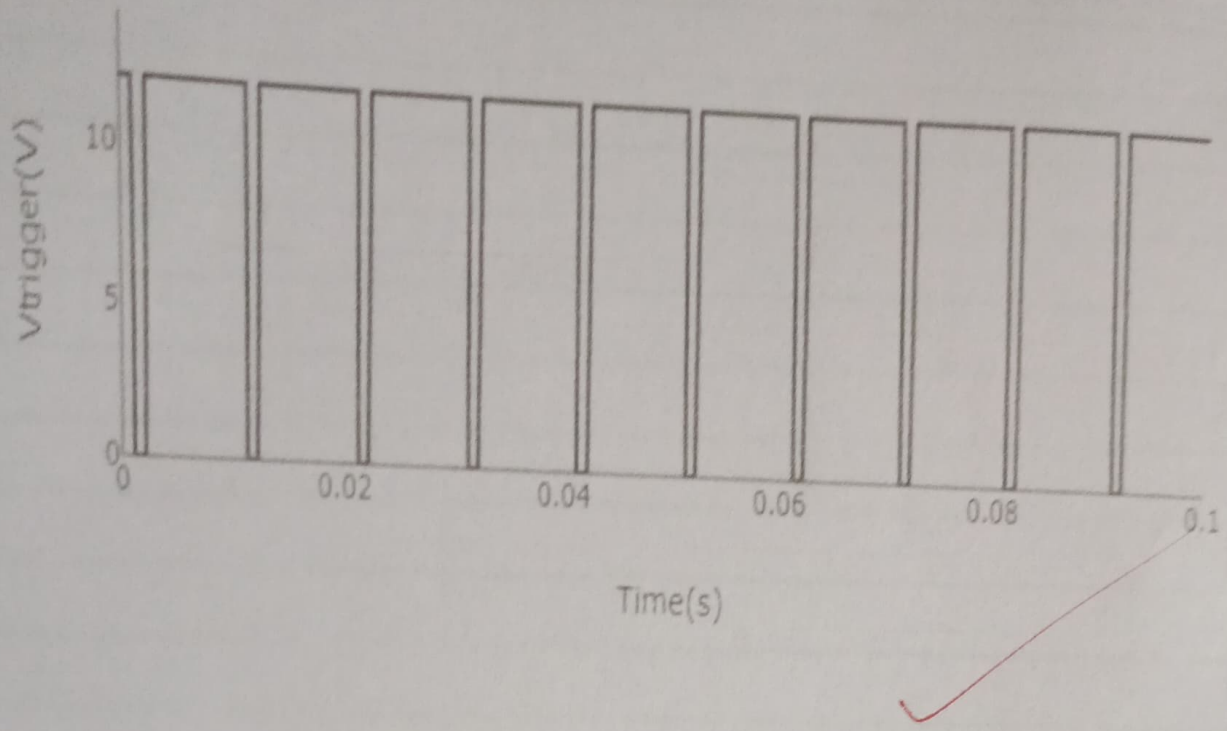
[Least Count = 1 milisecond]

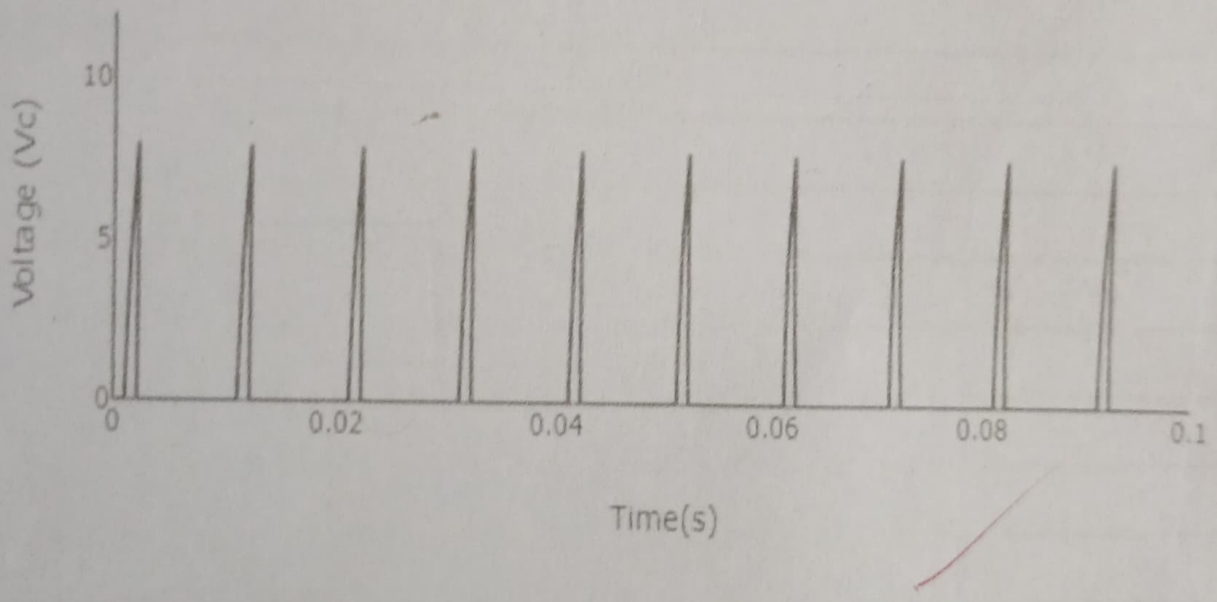
ASTABLE

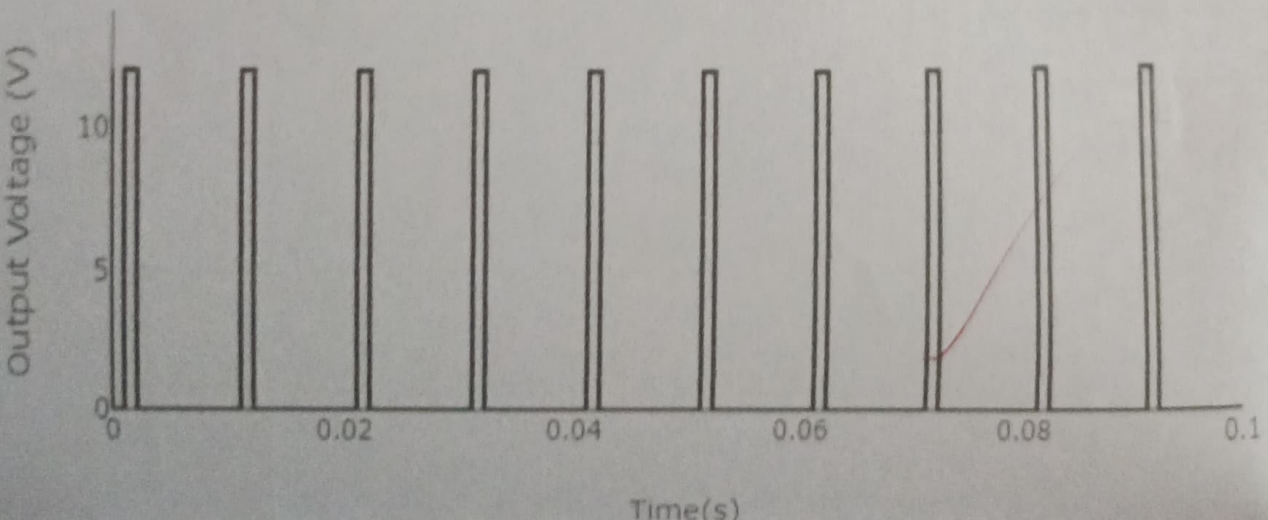

Voltage (Vc)
10
5
0
0
0.002
0.004
0.006
0.008
0.01
Time(s)


Output Voltage (V)
10
5
0
0
0.002
0.004
0.006
0.008
0.01
Time(s)

MONOSTABLE


Vtrigger(V)
10
5
0
0
0.02
0.04
0.06
0.08
0.1
Time(s)


Voltage (Vc)
10
5
0
0
0.02
0.04
0.06
0.08
0.1
Time(s)


Output Voltage (V)
10
5
0
0
0.02
0.04
0.06
0.08
0.1
Time(s)

Experiment :

Date 5/11/24

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Experiment-7

Inverting and non Inverting Amplifiers

* Aim- To study the basic properties of op-amp (Inverting and non-Inverting amp)

* Apparatus- Op-Amp, resistor, connecting wires, oscilloscope

* Theory Op-Amp is a linear electronic device having 3 terminals. It can perform multiple functions when attached to different feedback combinations. It is generally used as voltage amplifier.

(1) Inverting Op-Amp :-

Open loop gain (A_o) of Op-Amp is very high making it unstable, so to make it stable with a controllable gain, feedback is applied through some external resistor (R_f) from its output to inverting output terminal. The non-inverting terminal of Opamp is grounded.

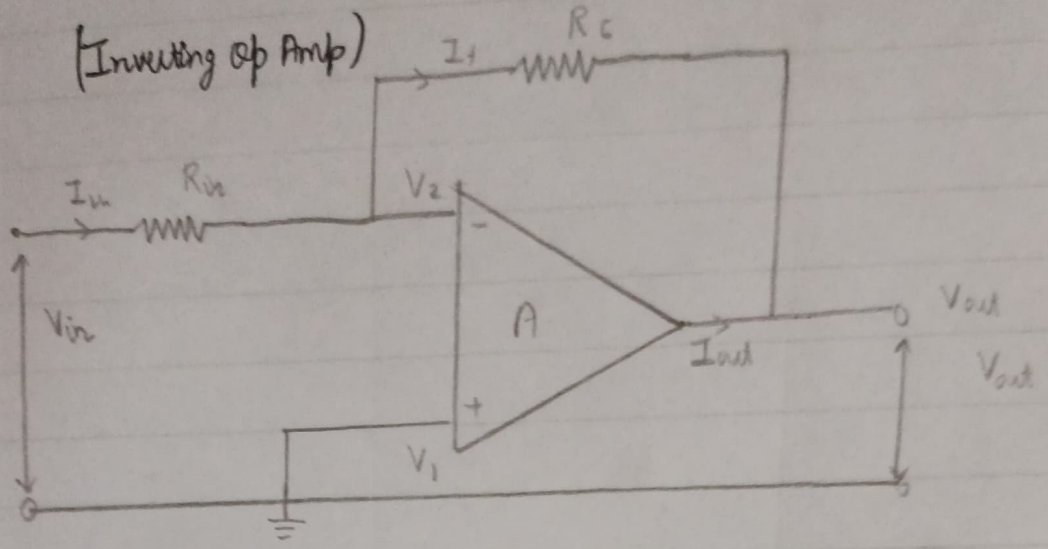
$$I = \left(\frac{V_{in} - V_{out}}{R_{in} + R_F} \right)$$

$$I = \frac{V_{in}}{R_{in}} - \frac{V_-}{R_{in}} = \frac{V}{R_F} - \frac{V_{out}}{R_F}$$

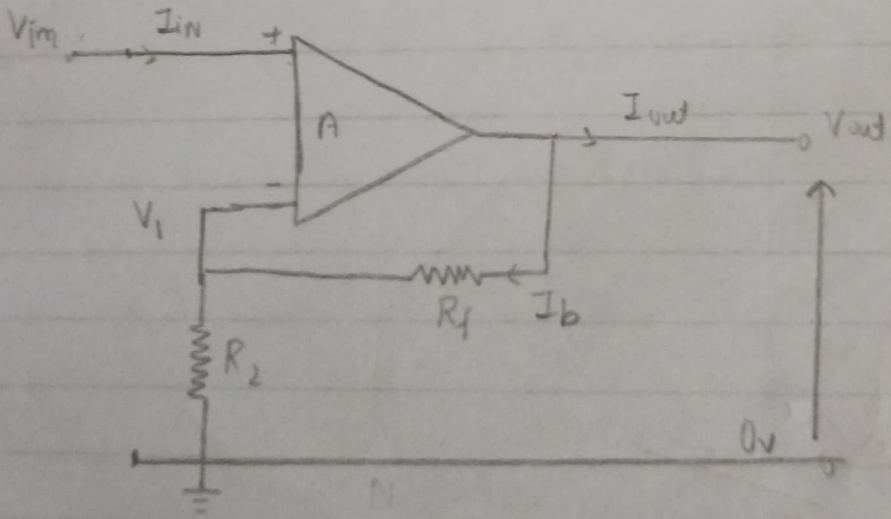
$$I = \left(\frac{V_{in} - 0}{R_{in}} \right) = \left(\frac{0 - V_{out}}{R_F} \right)$$

→ Diagram

(Inverting Op Amp)



(Non. Inverting Op-Amp)



Experiment :

Date

Page No.

$$V_{out} = \frac{-R_F}{R_{in}} \times V_{in}$$

$$A_{cl} = \frac{V_{out}}{V_{in}} = \frac{-R_F}{R_{in}}$$

(2) Non - inverting op-amp

In this config, input signal is directly fed to non inverting terminal where feedback is negative ; gain is positive and output voltage in phase with inputs as compared to inverting op-amp where gain is negative, output voltage is out of phase with input. This layout of inverting terminal make R_f and R_2 a potential divider, hence, determines gain of circuit.

$$V_{in} = \frac{R_2}{R_2 + R_f} \times V_{out}$$

$$A_{cl} = \frac{V_{out}}{V_{in}} = \frac{R_2 + R_f}{R_2} = 1 + \frac{R_f}{R_2}$$

$$V_{out} = \left[1 + \frac{R_f}{R_2}\right] * V_{in}$$

* Precautions-

1) Ensure all connections are secure and correct before powering on circuit.
2) Verify power supply voltage matches op amp specifications
3) Ensure proper grounding

Observation Table

(1) Inverting Op Amp ($R_1 = 10\,\Omega$, $R_f = 2\,\Omega$)

S.No	Input Voltage (V)	Output Voltage (V)	Current (mA)
1	-15	3	-0.176
2	-10	2	-0.118
3	-5	1	-0.0588
4	0	0	0
5	5	-1	0.0588
6	10	-2	0.118
7	15	-3	0.176

2) Non Inverting Op-Amp ($R_1 = 10\,\Omega$, $R_f = 2\,\Omega$)

S.No	Input Voltage (V)	Output Voltage (V)	Current (mA)
1	-15	-18	-0.324
2	-10	-12	-0.216
3	-5	-6	-0.108
4	0	0	0
5	5	6	0.107
6	10	12	0.216
7	15	18	0.324

Experiment :

Date

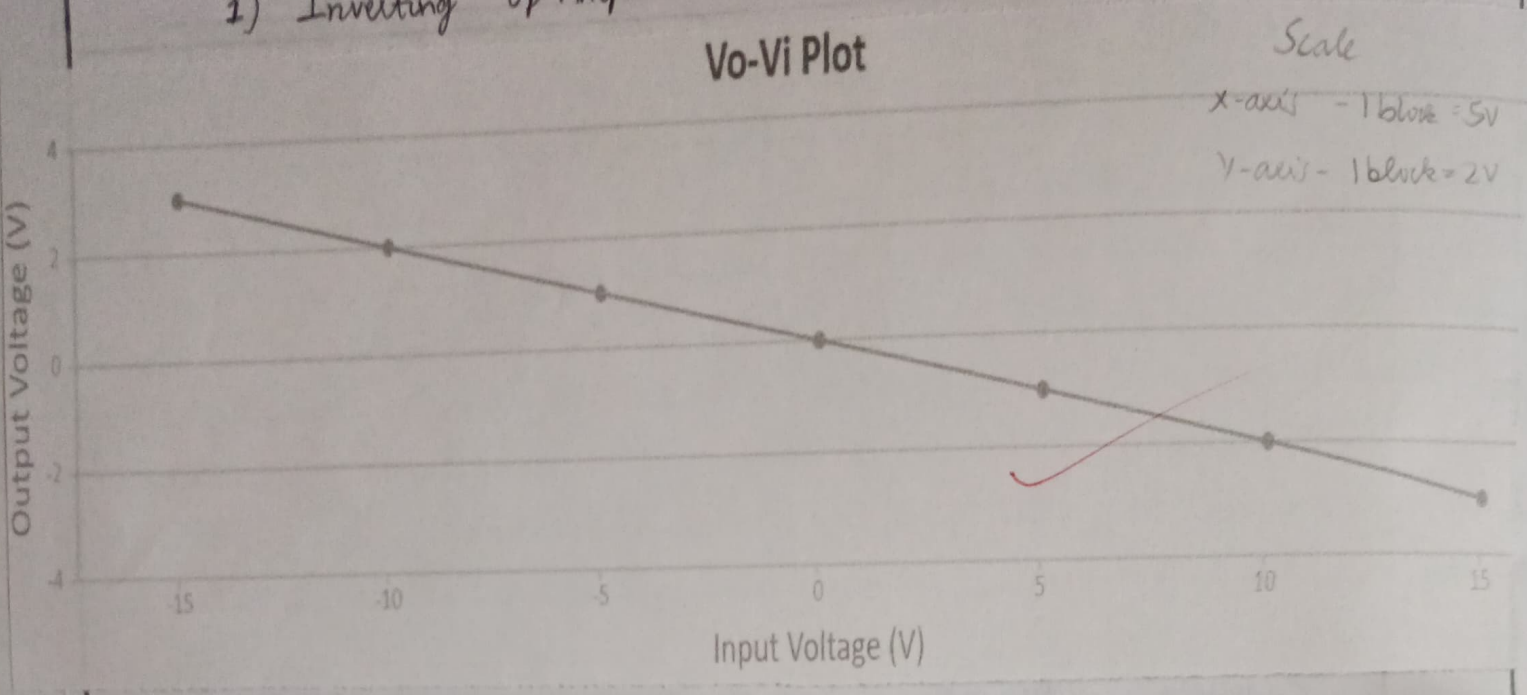
Page No.

Conclusion

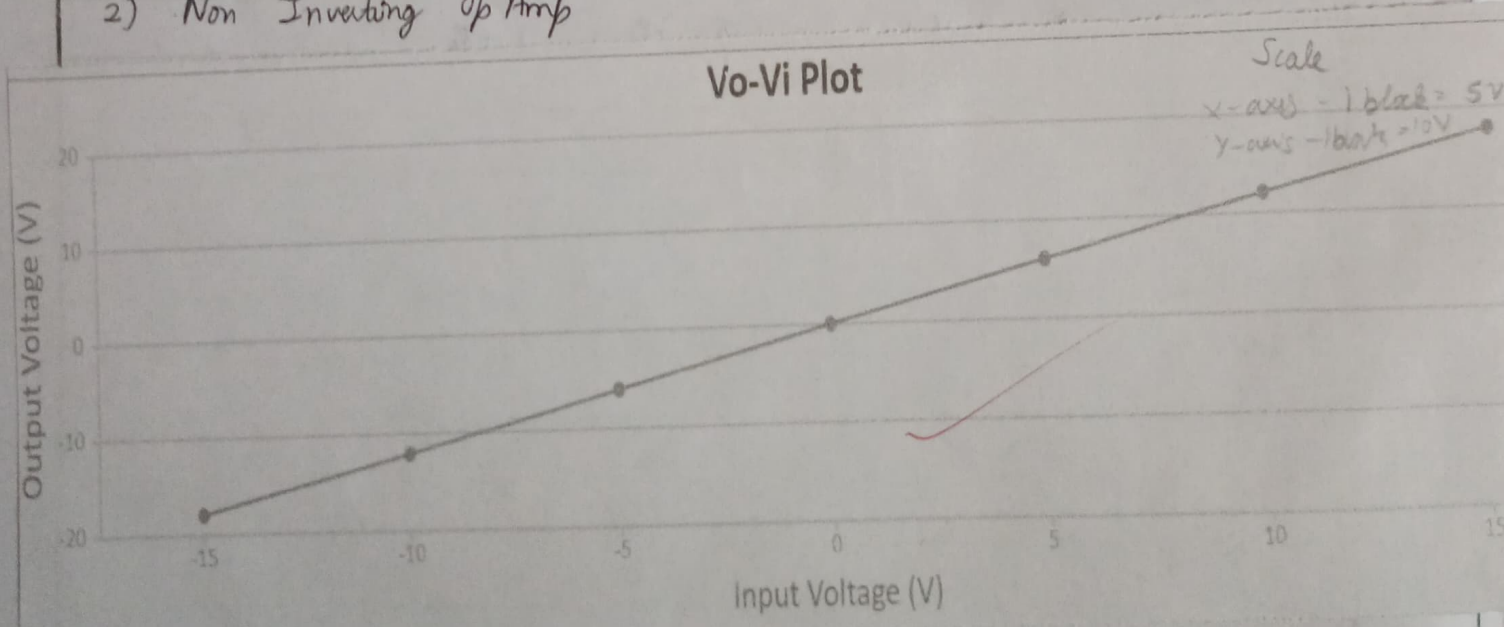
The experiment on the basic prop of op-amp provided a clear understanding of their functionality. By analyzing their gain, input and output behaviours we observed how signal inversion and amplification depend on circuit design. The inverting amp showed phase reversal with gain by external resistor, while non-inverting maintained phase and offered higher inp impedance

* GRAPHS

1) Inverting Op Amp



2) Non Inverting Op Amp



Experiment :

Date 12/11/24
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Experiment-8

Differentiator and Integrator using Op-Amp

 # Aim- To study Differentiator and integrator using op-amp.

 # Apparatus- Op-amp, Connecting wires, resistors, oscilloscope, capacitor

 # Theory

Op amp is a linear electronic device having three terminals, 2 high impedance input and one output terminal. Op-amp can perform multiple function when attached to different feedback combinations Generally, used as one voltage amplifier.

1) The Integrator

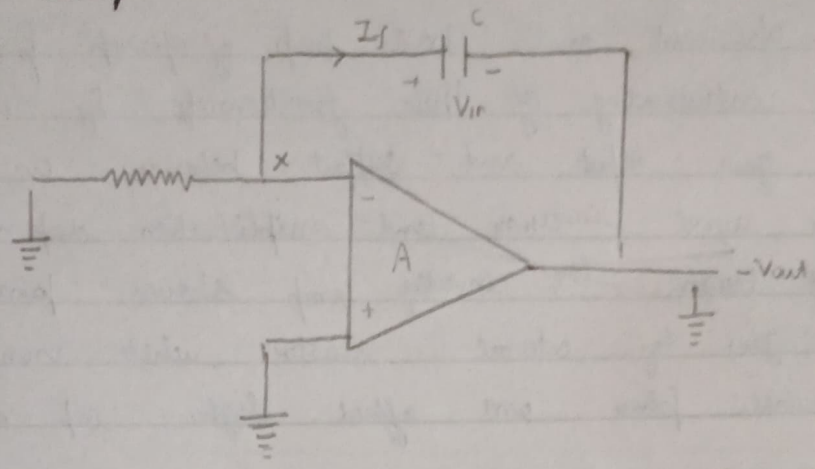
Its a circuit designed with op-amp so that it performs mathematical integration operation. Its output is proportional to amplitude and time duration of input. Feedback resistor replaced by capacitor. The results in ratio of capacitor impedance and input resistance increasing causing a linearly increasing amp output voltage that continues to increase until capacitor becomes fully charged.

$$V_c = \frac{Q}{C} \qquad I_{in} = \frac{V_{IN} - 0}{R_{IN}}$$

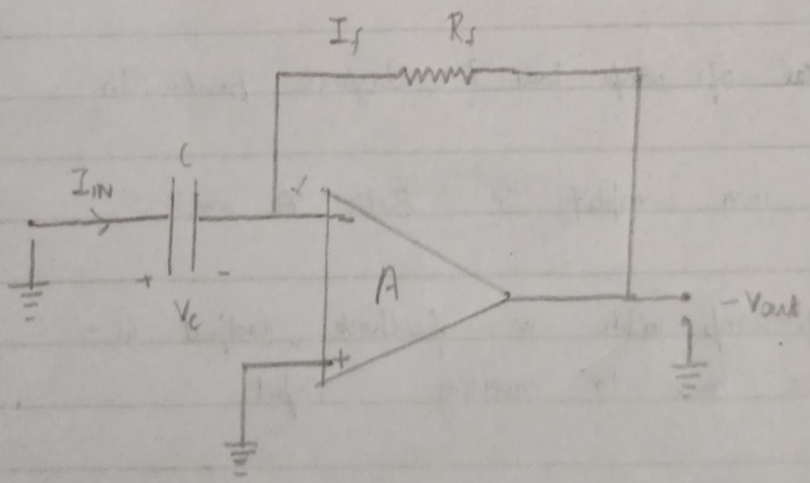
CLASSTIME

※ Diagram

(1) The Integrator



(2) The differentiator



Experiment :

Date

Page No.

$$I_f = C \times \frac{\partial V_{out}}{\partial t} = C \times \frac{1}{C} \times \frac{dQ}{dt} = \frac{dQ}{dt}$$

$$\text{So, } V_{out} = \frac{-1}{R_{IN} \times C} \int V_{in}\, dt$$

$$V_{out} = \frac{-1}{j \times \omega R_{IN} \times C} \times V_{IN}$$

2) The differentiator

In differentiation circuit, input is connected to inverting output of op-amp through C and negative feedback is applied to inverting input through R_f. Circuit provides mathematical differentiation operation and output is first derivative of input signal

$$I_{IN} = I_C = \frac{-V_{out}}{R_f}$$

$$I_f = C \times \frac{\partial V_{IN}}{\partial t} = I_{IN}$$

$$\frac{-V_{out}}{R_f} = C \times \frac{dV_{IN}}{dt}$$

$$V_{out} = -R_f \times C \times \frac{\partial V_{IN}}{dt}$$

** Precaution :-

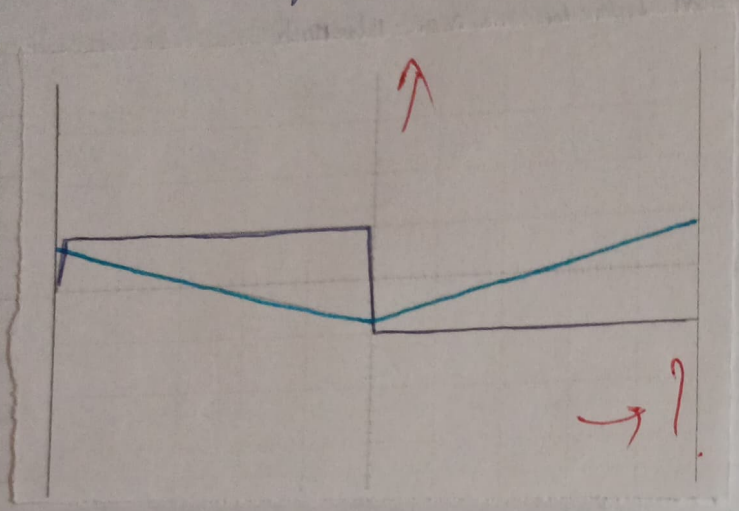
1) Verify the power supply voltage meter op-amp
2) Ensure proper grounding to prevent noise.
3) Avoid overheating by proper ventilation

CLASSTIME

[Light blue – Input waveform
Blue – Output waveform]

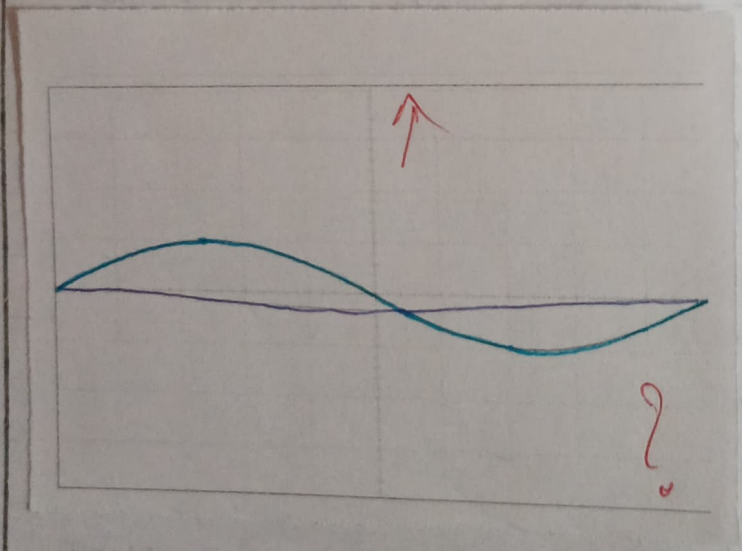
* GRAPH

① Integrator



(a) Square wave
freq = 3000Hz
Amplitude = 0.5 V

(b) Sine wave



freq = 3000Hz
Amplitude = 0.5V

Experiment :

Date

Page No.

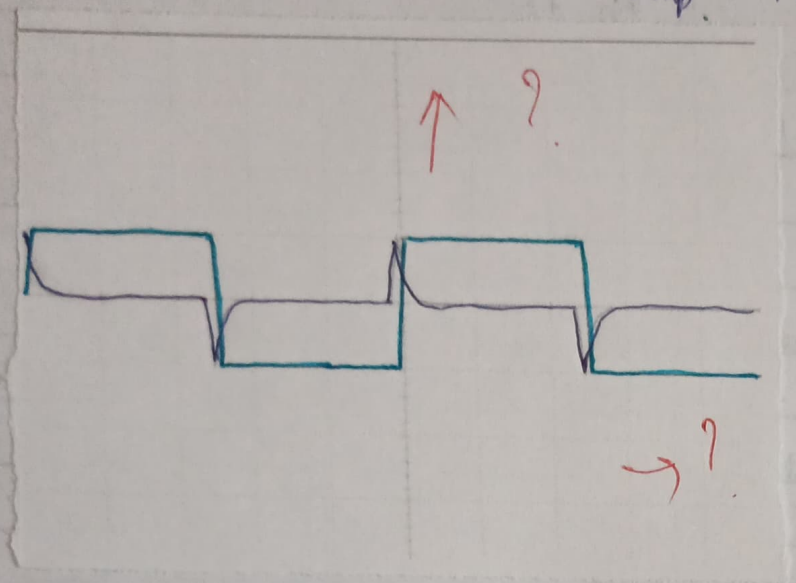
Conclusion

The experiment on differentiator and integrator circuits using op-amp demonstrated their functionality in signal processing. The differentiator does mathematical differentiation and integrator does mathematical integration. The practical implementation validated the theoretical concepts by observing expected phase shifts and waveform

GRAPHS

② Differentiator

a) Square wave → freq = 2000Hz
Amp = 1V



(b) Sine wave freq = 2000Hz
Amp = 1V